

CLAIMS

1 1. A surface channel MOSFET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h;
4 a Si channel layer;
5 a gate dielectric;
6 a polycrystalline semiconductor layer; and
7 a highly conductive gate layer.

1 2. The MOSFET of claim 1, wherein h is approximately 0.

1 3. The MOSFET of claim 1, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 4. The MOSFET of claim 1, wherein the substrate comprises Si.

1 5. The MOSFET of claim 1, wherein the substrate comprises Si with a layer of SiO_2 .

1 6. A surface channel MOSFET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h;
4 a Ge channel layer;
5 a Si layer;
6 a gate dielectric;
7 a polycrystalline semiconductor layer; and

8 a highly conductive gate layer.

1 7. The MOSFET of claim 6, wherein h is approximately 0.

1 8. The MOSFET of claim 6, wherein the thickness of the Si layer is less than 5nm.

1 9. The MOSFET of claim 6, wherein the substrate comprises relaxed graded

2 composition SiGe layers on Si.

1 10. The MOSFET of claim 6, wherein the substrate comprises Si.

1 11. The MOSFET of claim 6, wherein the substrate comprises Si with a layer of SiO₂.

1 12. A buried channel MOSFET comprising:

2 a relaxed planarized SiGe layer on a substrate;

3 a regrown Si_{1-x}Ge_x layer with thickness h;

4 a Si channel layer;

5 a Si_{1-y}Ge_y layer;

6 a second Si layer;

7 a gate dielectric;

8 a polycrystalline semiconductor layer; and

9 a highly conductive gate metal layer.

1 13. The MOSFET of claim 12, wherein h is approximately 0.

1 14. The MOSFET of claim 12, wherein the thickness of the second Si layer is less than

2 5nm.

1 15. The MOSFET of claim 12, wherein supply layer dopants are located in the $\text{Si}_{1-y}\text{Ge}_y$
2 layer.

1 16. The MOSFET of claim 15, wherein the supply layer dopants are implanted.

1 17. The MOSFET of claim 12, wherein the supply layer dopants are located below the
2 Si channel layer.

1 18. The MOSFET of claim 17, wherein the supply layer dopants are implanted.

1 19. The MOSFET of claim 12, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 20. The MOSFET of claim 12, wherein the substrate comprises Si.

1 21. The MOSFET of claim 12, wherein the substrate comprises Si with a layer of
2 SiO_2 .

1 22. A buried channel FET comprising:

2 a relaxed planarized SiGe layer on a substrate;

3 a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h;

4 a Si channel layer;

5 a $\text{Si}_{1-y}\text{Ge}_y$ layer;

6 a second Si layer; and

7 a highly conductive gate layer.

1 23. The FET of claim 22, wherein h is approximately 0.

1 24. The FET of claim 22, wherein the thickness of the second Si layer is less than
2 5nm.

1 25. The FET of claim 22, wherein supply layer dopants are located in the $\text{Si}_{1-y}\text{Ge}_y$
2 layer.

1 26. The FET of claim 25, wherein the supply layer dopants are implanted.

1 27. The FET of claim 22, wherein the supply layer dopants are located below the Si
2 channel layer.

1 28. The FET of claim 27, wherein the supply layer dopants are implanted.

1 29. The FET of claim 22, wherein the substrate comprises relaxed graded composition
2 SiGe layers on Si.

1 30. The FET of claim 22, wherein the substrate comprises Si.

1 31. The FET of claim 22, wherein the substrate comprises Si with a layer of SiO_2 .